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Today's Date: 7/11/07 Date Needed by: _____ **RUSH – SPE signature** _____

Your Name Michael Horabik

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Room # Jeff-21069 Phone 2 3068

Serial # _____
Priority Date 10/7/05

Format for Search Results: PAPER   EMAIL

Where have you searched?
EAST _____
NPL _____ where - IEEE, ACM, internet, other

DESCRIBE the scope of your request, such as the area of art, novelty, process or method if applicable. Specify the concepts, synonyms, keywords, acronyms, or definitions and the relationship of the concepts to each other. Please attach a copy of the backgound, abstract, and pertinent claims of the application. **ONLY specifying CLAIM 1 is not enough.**

US 5903260

STIC Searcher KaS Phone 2-4235
Date picked up 7/11/07 Date completed 7/11/07
DATABASES Searched Questel /Lexis /Corinth TEXT _____ LITIGATION X
OTHER _____

sira
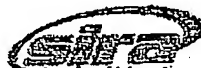
1 / 1 FAMPAT - ©QUESTEL-ORBIT - image

FAN - 20042770378974

PN - ⚐ US5903260 A 19990511 [US5903260]

TI - Flat panel device and display driver with on/off power controller used to prevent damage to the LCD

PA - SEIKO EPSON CORP

PA0 - Seiko Epson Corporation, Tokyo [JP]

IN - IMAMURA YOUICHI

AP - 1996US-0582771 19960102

FD - (US5903260)
Divsn of US267103 19940623 [1994US-0267103]
Cont. of US834295 19920409 [1992US-0834295] (Abandoned)
Division of: US5563624

PR - 1990JP-0159416 19900618; 1991WO-JP00785 19910611; 1992US-0834295 19920409; 1994US-0267103 19940623
1996US-0582771 19960102

IC - G05B-011/01
G06F-003/147
G09G-003/20
G09G-003/36
G09G-005/00

ICAA - G06F-003/147 [2006-01 A - I R M EP]; G09G-003/20 [2006-01 A - I R M EP]; G09G-003/36 [2006-01 A - I R M EP]

ICCA - G06F-003/147 [2006 C - I R M EP]; G09G-003/20 [2006 C - I R M EP]; G09G-003/36 [2006 C - I R M EP]

EC - G06F-003/147
G09G-003/20
G09G-003/36C12P
G09G-003/36C16

PCL - ORIGINAL (O) : 345211000; CROSS-REFERENCE (X) : 700012000

CT - (US5903260)
US3947811; US4268827; US4314245; US4453208; US4541066; US4674031; US4687956; US4748444; US4758896; US4855892; US4922448; US4931791; US5077553; US5155477; US5155613; US5592191; US5629715; US5710929; EP162969; EP326158; EP419910; JP49-97593; JP100997; JP128178; JP55-117190; JP123118; JP6150195

AB - (US5903260)
Signal management control units 471-47n of respective scan drivers LSI in an LCD module are cascade-connected and each have the same construction. A detected signal of the signal management control unit 47J is a data signal latch clock LP applied to a terminal CKB1. A detected signal of the signal management control unit 472 is a frame start signal SP applied to a terminal CKB2. A detected signal of the signal management control unit 47n is an AC-transforming clock FR applied to a terminal CKBn. The signal management control unit 471 includes a signal stop detection circuit 48 serving as a signal

detection means for detecting a stop of the detected signal and a sequence processing circuit 51 consisting of a signal delay circuit 49 and a logic circuit 50. When stopping oscillations of, e. g., the frame start signal SP, outputs T1-Tn of the circuit 51 change to an L level. Hence, a display-off signal DF of the LCD module assumes the L level. A liquid crystal panel is forcibly set in a display-off mode. As a result, even if the frame start signal SP is stopped due to some cause, a liquid crystal application voltage is set down to zero. It is, therefore, possible to avoid a liquid crystal DC drive and prevent a deterioration of the liquid crystal.

OBJ - (US5903260)

The present invention relates generally to a flat display such as liquid crystal display (LCD) and plasma display panels and also applied devices thereof, and more particularly, to a flat display device having such a configuration that a display body module and a display control unit for controlling the display are separately disposed as well as to a display body driving device.

Accordingly, it is an object of the present invention devised in light of the above-described problems to provide a flat display device and a display body driving device which are capable of preventing deterioration of display characteristics due to a DC drive of a display panel, this deterioration being derived from an abnormality of a signal supplied from a display control unit to a display body module unit.

ADB - (US5903260)

As a result, even if the frame start signal SP is stopped due to some cause, a liquid crystal application voltage is set down to zero.

Deterioration of the liquid crystal display panel 22 is caused which is more expensive than other parts and therefore difficult to exchange.

This is a serious problem to the display device based on visual recognizability.

ICLM - (US5903260)

1. A method of controlling a flat display unit comprising a flat display panel driven in accordance with display driving voltages, display driver means for selecting the display driving voltages supplied to the flat display panel and a display power source circuit for supplying the display driving voltages to the display driver means in response to a power control signal, the method of controlling the flat display unit comprising the steps of:

detecting a logic power voltage activating a logic circuit of the flat display unit by the display driver means;

supplying the power control signal from the display driver means to the power source circuit, said power control signal having a delay time after the detection of said logic power voltage;

supplying the display driving voltages to the display driver means in response to the power control signal by the power source circuit; and

selecting the display driving voltages supplied from the power source circuit to the flat display panel by the display driver means.

3. A method of controlling a flat display device comprising a flat display panel module unit and a display control unit for supplying control signals to control display of the flat display panel module unit; said flat display panel module unit including a flat display panel driven in accordance with display driving voltages, display driver means for selecting the display driving voltages to the flat display panel and a display power source circuit for supplying the display driving voltages to the display driver means in response to a power control signal, the method of controlling the flat display unit comprising the steps of:

supplying the power control signal to the power source circuit by the display driver means, the power control signal having a delay time after a logic power voltage has been supplied to a logic circuit of the flat display device; supplying the display driving voltages to the display driver means in response to the power control signal by the power source circuit; supplying a display start signal controlling a start of the selection of the display driving voltages by the display driver means in response to the control signal supplied from the display control unit, said display start signal having a delay time after the power control signal has supplied to the power source circuit; and selecting the display driving voltages supplied from the power source circuit to supply to the flat display panel in response to the display start signal.
5. A flat display unit comprising:
a flat display panel for being driven in accordance with display driving voltages; display driver means for selecting the display driving voltages supplied to said flat display panel, said display driver means comprising a logic circuit and a detection means for detecting a logic power voltage, activating said logic circuit and for supplying a power control signal having a delay time after the detection of the logic power voltage; and
a display power source circuit for supplying the display driving voltages to said display driver means in response to the power control signal.
6. A flat display device comprising a flat display panel module unit and a display control unit for supplying control signals to control display of the flat display panel module unit,
said flat display panel module unit comprising:
- a flat display panel driven in accordance with display driving voltages;
- display driver means for selecting the display driving voltages supplied to said flat display panel and for supplying a power control signal having a delay time after a logic power voltage has been supplied to a logic circuit of said display driver means; and
- a display power source circuit for supplying the display driving voltages to said display driving means in response to the power control signal,
- wherein said display driver means starts the selection of the display driving voltages in response to a display start signal having a delay time after the power control signal has supplied to said power source circuit.

UP   -   2000-08

UP - 2004-20

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1 / 1 CRXX - ©CLAIMS/RRX

PN -   5,903,260 A 19990511 [US5903260]

PA - Seiko Epson Corp JP

ACT - 20010511 REISSUE REQUESTED
ISSUE DATE OF O.G.: 20011009
REISSUE REQUEST NUMBER: 09/854349
EXAMINATION GROUP RESPONSIBLE FOR REISSUEPROCESS: 2775
Reissue Patent Number: USRE39236

20031001 REISSUE REQUESTED
ISSUE DATE OF O.G.: 20040511
REISSUE REQUEST NUMBER: 10/677165
EXAMINATION GROUP RESPONSIBLE FOR REISSUEPROCESS: 2675

Reissue Patent Number:

Search statement   2

UNITED STATES PATENT AND TRADEMARK OFFICE GRANTED PATENT

5903260

May 11, 1999

Flat device and display driver with on/off power controller
used to prevent damage to the LCD

REISSUE: May 11, 2001 - Reissue Application filed Ex. Gp.: 2775; Re. S.N.
09/854,349 (O.G. October 9, 2001)
October 1, 2003 - Reissue Application filed Ex. Gp.: 2675; Re. S.N. 10/677,165
(O.G. May 11, 2004)
August 14, 2007 - This patent was reissued as Reissue Patent RE 39,236 (O.G.
August 14, 2007)

APPL-NO: 582771   (08)

FILED-DATE: January 2, 1996

GRANTED-DATE: May 11, 1999

CORE TERMS: sub, display, liquid crystal, driver, scan, voltage, power source,
driving, module, terminal ...

5,903,260 OR 5903260

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